IN THE CLAIMS

Please replace all prior versions, and listings, of claims in the application with the following list of claims:

1. (Currently Amended) An arithmetic unit for multiplying a first quantity X by a second quantity Y, said arithmetic unit comprising:

a Booth coder having a plurality of inputs for receiving a plurality of bits of the second quantity and a plurality of outputs for providing Booth coded outputs; ~~and~~

circuitry connected to at least one of said inputs for receiving one of said plurality of bits of the second quadrant and said outputs for providing Booth coded outputs;

said circuitry comprising a further input to receive a signal indicating if a multiply accumulate or multiply subtract function is to be performed, said circuitry arranged to modify ~~modifying~~ at least one output of the coder[[,]] if necessary in accordance with said signal, whereby the output of said Booth coder unit is a Booth coded signal modified if necessary to take into account the unction to be performed wherein said coder is arranged to provide a SIFL output, an NZP output and an NZN output;

wherein said unit is capable of performing the calculations X multiplied by Y and X multiplied by Y, the output of the Booth coder being the same for both of said calculations; and

a Booth decoder arranged to separate a partial product from said Booth coded signal and said first quantity.

2. (Original) A unit as claimed in claim 1, wherein the Booth Coder comprises three inputs.

3. (Original) A unit as claimed in claim 1, wherein the Booth coder provides three outputs.

4. (Original) A unit as claimed in claim , 1 wherein said circuitry comprises a logic gate.

5. (Original) A unit as claimed in claim 4, wherein said logic gate is an exclusive OR gate.

6. (Canceled)

7. (Canceled)

8. (Original) A unit as claimed in claim 1, wherein said circuitry comprises at least one multiplexer.

9. (Canceled)

10. (Currently Amended) A unit as claimed in claim [[9]] 8, wherein said NZP and said NZN outputs are connected to said circuitry.

11. (Original) A unit as claimed in claim 10, wherein said NZP output is connected to a first and a second multiplexer and said NZN output is also connected to said first and second multiplexers.

12. (Original) A unit as claimed in claim 11, wherein a partial product is to be output, the first multiplexer provides the NZP output and the second multiplexer provides the NZN output and when the partial product of the opposite sign is to be generated, the first multiplexer provides the NZN output and the second multiplexer provides the NZP output.

13. (Original) A unit as claimed in claim 1, wherein said second quantity is a xN bit operand where x is an integer and N bits are used for multiplication with the first quantity, xN/2

Booth coders are provided and said circuitry is connected to inputs or outputs of said xN/2 Booth coders.

14. (Original) A unit as claimed in claim 13, wherein x is equal to two and the N most significant bits or the N least significant bits are used in said multiplication and said circuitry receives at least one control signal to control the selection of the N bits.

15. (Original) A unit as claimed in claim 12, wherein x is equal to two and the N most significant bits or the N least significant bits are used in said multiplication and said circuitry receives at least one control signal to control the selection of the N bits, three multiplexers are provided, the first and second multiplexers each receive the NZP and NZN outputs of first and second Booth coders and the third multiplexer receives the SNGL outputs of first and second Booth coders.

16. (Original) A unit as claimed in claim 1, wherein said circuitry is connected to at least two of said inputs.

17. (Currently Amended) A unit as claimed in claim 1, wherein one of said inputs <u>for receiving a one of said plurality of bits of the second quantity</u> to said Booth coder is a carry input.

18. (Currently Amended) A unit as claimed <u>in claim</u> ~~claims~~ 1, wherein said circuitry is arranged to receive a carry input.

19. (Original) A unit as claimed in claim 1, wherein said unit is arranged to provide a multiply accumulate or a multiply subtract function, said circuitry causing the partial product to be provided if the multiply accumulate function is to be provided and the partial product of the opposite sign if the multiply subtract function is to be provided.

20. (Original) A unit as claimed in claim 19, wherein a plurality of Booth coders are provided, one of said Booth coders being arranged to take into account a carry.

21. (Original) A unit as claimed in claim 20 wherein when a multiply subtract function is performed, the first value and the opposite of the second value are multiplied, where if the second value is Y, the opposite value is y+1, and +1 is the carry/

22. (Original) A unit as claimed in claim 19, wherein the output provided by said circuitry is arranged to provide an output which takes into account said carry, if required.

23. (Original) A unit as claimed in claim 1, wherein said circuitry is arranged to receive a control signal.

24. (Original) A unit as claimed in claim 1, wherein the modified output of said coder is decodable to a partial product opposite to the partial product decoded from the output prior to modification.